DLC Display Co., Limited

德爾西顯示器有限公司

MODEL No: DLC0154BNOG-W-2

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Record of Revision

Date	Revision No.	Summary
2015-01-22	1.0	Rev 1.0 was issued

1. Scope

This data sheet is to introduce the specification of DLC0154BNOG-W-2, passive matrix OLED module. It is composed of an OLED panel, driver ICs. The 1.54'' display area contains 128 x 64 pixels.

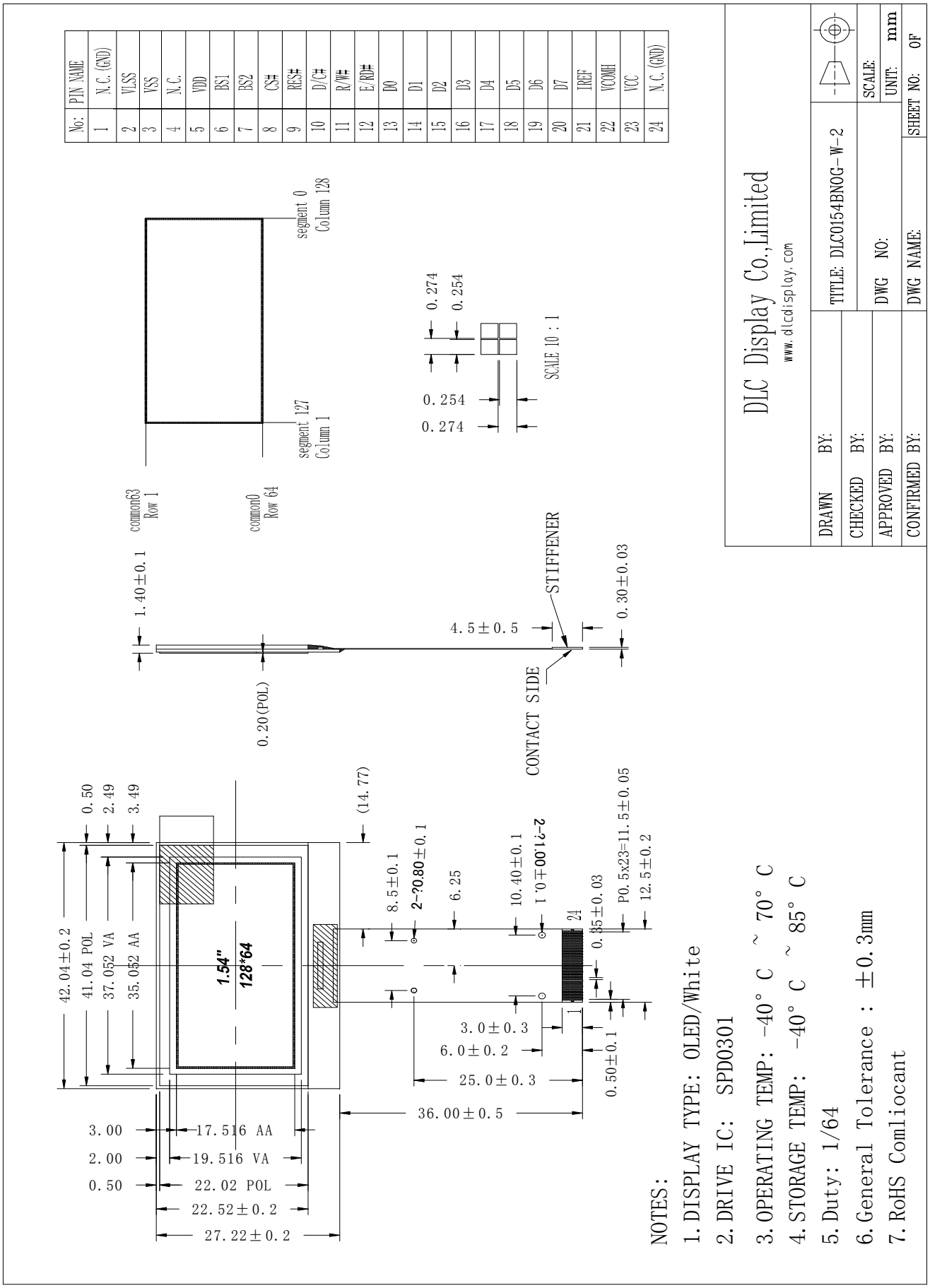
2. Application

Digital equipments which need display, instrumentation, remote control, electronic product.

3. General Information

Item	Contents	Unit
Size	1.54	inch
Resolution	128×64	/
Display Color	Monochrome (White)	/
Interface	8-bit 68XX/80XX Parallel, 4-wire SPI, I2C	/
Dot Size (W×H)	0.254 × 0.254	mm
Pixel pitch (W×H)	0.274 × 0.274	mm
Outline Dimension(W x H x D)	42.04 × 27.22 × 1.40	mm
Active Area (W×H)	35.052 × 17.516	mm
Driver IC	SPD0301	/
Drive Duty	1/64 Duty	/
Operating Temperature	-40℃~+70℃	
Storage Temperature	-40℃~＋85℃	
Weight	TBD	g

4. Outline Drawing



5. Interface signals

<table>
<tr><th>Pin Number</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td>1</td><td>N.C.
(GND)</td><td>-</td><td>Reserved Pin (Supporting Pin)
The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground as the ESD protection circuit.</td></tr>
<tr><td>2</td><td>VLSS</td><td>P</td><td>Ground of Analog Circuit
This is an analog ground pin. It should be connected to VSS externally.</td></tr>
<tr><td>3</td><td>VSS</td><td>P</td><td>Ground of Logic Circuit
This is a ground pin. It also acts as a reference for the logic pins. It must be connected to external ground.</td></tr>
<tr><td>4</td><td>N.C.</td><td>-</td><td>Reserved Pin (Supporting Pin)
The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground as the ESD protection circuit.</td></tr>
<tr><td>5</td><td>VDD</td><td>P</td><td>Power Supply for Logic Circuit
This is a voltage supply pin. It must be connected to external source.</td></tr>
<tr><td>6
7</td><td>BS2
BS1</td><td>I</td><td>Communicating Protocol Select
These pins are MCU interface selection input. See the following table:
<table>
<tr><td></td><td>68XX-parallel</td><td>80XX-parallel</td><td>I2C</td><td>4-wire SPI</td></tr>
<tr><td>BS1</td><td>0</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>BS2</td><td>1</td><td>1</td><td>0</td><td>0</td></tr>
</table></td></tr>
<tr><td>8</td><td>CS#</td><td>I</td><td>Chip Select
This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.</td></tr>
<tr><td>9</td><td>RES#</td><td>I</td><td>Power Reset for Controller and Driver
This pin is reset signal input. When the pin is low, initialization of the chip is executed. Keep this pin pull high during normal operation</td></tr>
<tr><td>10</td><td>D/C#</td><td>I</td><td>Data/Command Control
This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 is treated as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.
When the pin is pulled high and serial interface mode is selected, the data at SDIN is treated as data. When it is pulled low, the data at SDIN will be transferred to the command register. In I2C mode, this pin acts as SA0 for slave address selection.</td></tr>
<tr><td>11</td><td>R/W#</td><td>I</td><td>Read/Write Select or Write
This pin is MCU interface input. When interfacing to a68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to “High” for read mode and pull it to “Low” for write mode.</td></tr>
</table>

			When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low.
12	E/RD#	I	*Read/Write Enable or Read* This pin is MCU interface input. When interfacing to a68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low. When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low. When serial or I2C mode is selected, this pin must be connected to VSS.
13~20	D7~D0	I/O	*Host Data Input/Output Bus* These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK. When I2Cmode is selected, D2 & D1 should be tired together and serve as SDA out & SDA in application and D0 is the serial clock input SCL. Unused pins must be connected to VSS except for D2 in serial mode.
21	IREF	I	*Current Reference for Brightness Adjustment* This pin is segment current reference pin. A resistor should be connected between this pin and VSS. Set the current at 12.5uA maximum.
22	VCOMH	I	*Voltage Output High Level for COM Signal* This pin is the input pin for the voltage output high level for COM signals. A capacitor should be *connected* between this pin and VSS.
23	VCC	P	*Power Supply for OEL Panel* This is the most positive voltage supply pin of the chip. A stabilization capacitor should be connected between this pin and VSS when the converter is used. It must be connected to external source when the converter is not used.
24	N.C. (GND)	-	*Reserved Pin (Supporting Pin)* The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground as the ESD protection circuit.

6. Absolute maximum Ratings

6.1. Electrical Absolute max. ratings

Parameter	Symbol	MIN	MAX	Unit	Remark
Supply Voltage	VDD	-0.3	4.0	V	1,2
Driver supply voltage	VCC	8	17	V	

Note 1: All the above voltages are on the basis of “VSS = 0V”.

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 7 and 9 “Optical & Electrical Characteristics”. If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

6.2. Environment Conditions

Item	Symbol	MIN	MAX	Unit	Remark
Operating Temperature	TOPR	-40	70	℃	
Storage Temperature	TSTG	-40	85	℃	

Note : The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80℃.

7. Electrical Specifications

7.1 Electrical characteristics

GND=0V, Ta=25℃

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Supply Voltage for Logic	VDD	1.7	1.8	1.9	V	
		2.7	2.8	2.9	V	
Supply Voltage for Display	VCC	11.5	12.0	12.5	V	Note 1
Input Signal Voltage	VIL	0	--	0.2×VDD	V	I_{OUT} = 100 A, 3.3MHz
	VIH	0.8×VDD	--	VDD	V	I_{OUT} = 100 A, 3.3MHz
output Signal Voltage	VOL	0	-	0.1×VDD	V	I_{OUT} = 100 A, 3.3MHz
	VOH	0.9×VDD	-	VDD	V	I_{OUT} = 100 A, 3.3MHz
VDD Supply Current VDD =2.8V, VCC = 12, IREF = 10uA , No Panel attached, Display ON, All ON	IDD	--	90	110	uA	Contrast = FFh
VCC Supply Current VDD = 2.8V, VCC =12, IREF =10uA, No Panel attached, Display ON, All ON	ICC	--	450	580	uA	
Sleep Mode Current for VDD	$I_{DD, SLEEP}$	-	-	10	uA	VDD = 1.65V~3.3V, VCC = 7V~16V Display OFF, No panel attached
Sleep Mode Current for VCC	$I_{CC, SLEEP}$	-	-	10	uA	
Segment Output Current, VDD = 2.8V, VCC =12V, IREF=10uA, Display ON.	I_{SEG}	280	310	340	uA	Contrast=FFh
		-	215	-	uA	Contrast=AFh
		-	155	-	uA	Contrast=7Fh
		-	78	-	uA	Contrast=3Fh
		20	-	-	uA	Contrast=0Fh

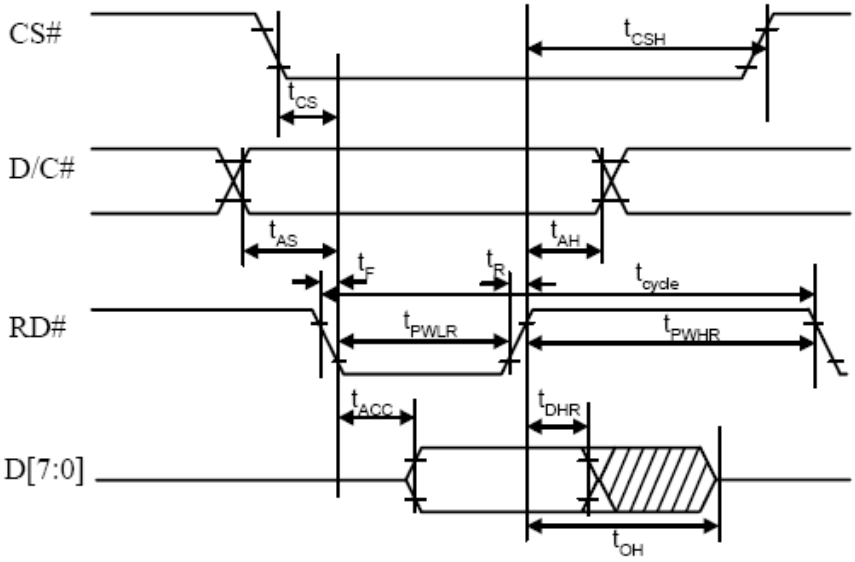
8. Command/AC Timing

8.1 AC Characteristics

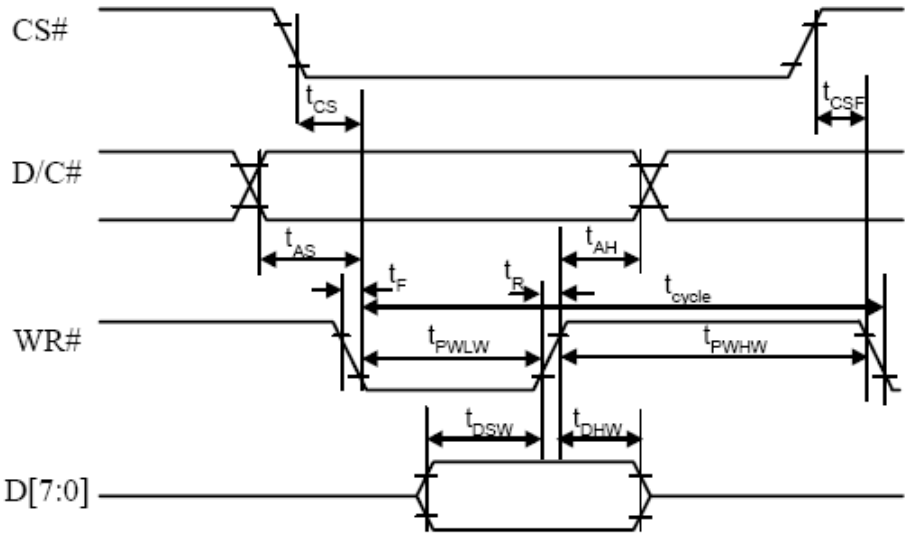
8.1.1 68XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
tcycle	System Cycle Time	300	-	ns
tAS	Address Setup Time	10	-	ns
tAH	Address Hold Time	0	-	ns
tDSW	Write Data Setup Time	40	-	ns
tDHW	Write Data Hold Time	7	-	ns
tDHR	Read Data Hold Time	20	-	ns
tOH	Output Disable Time	-	70	ns
tACC	Access Time	-	140	ns
PWCSL	Chip Select Low Pulse Width (Read)	120	-	ns
	Chip Select Low Pulse width (Write)	60		
PWCSH	Chip Select High Pulse Width (Read)	60	-	ns
	Chip Select High Pulse Width (Write)	60		
tR	Rise Time	-	15	ns
tF	Fall Time	-	15	ns

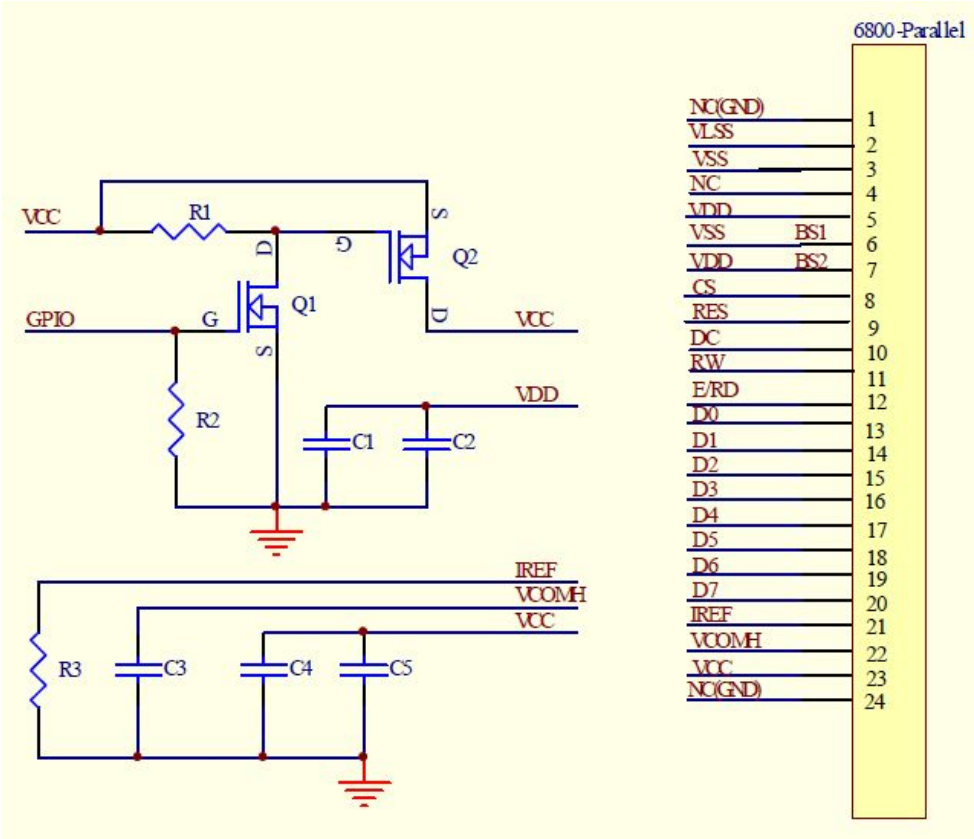
* (V_{DD} - V_{SS} = 1.65V to 3.3V, T_a = 25°C)



(Read Timing)



(Write Timing)



Recommended Components:

C1, C2: 1µF / 16V, X5R
C3: 2.2µF /25V
C4: 4.7µF / 25V, X7R
C5: 0.1µF/ 25V, X7R
R1, R2: 47kΩ
R3: 910KΩ, R3 = (Voltage at IREF - VSS) / IREF
Q2: FDN338P
Q1: FDN335N

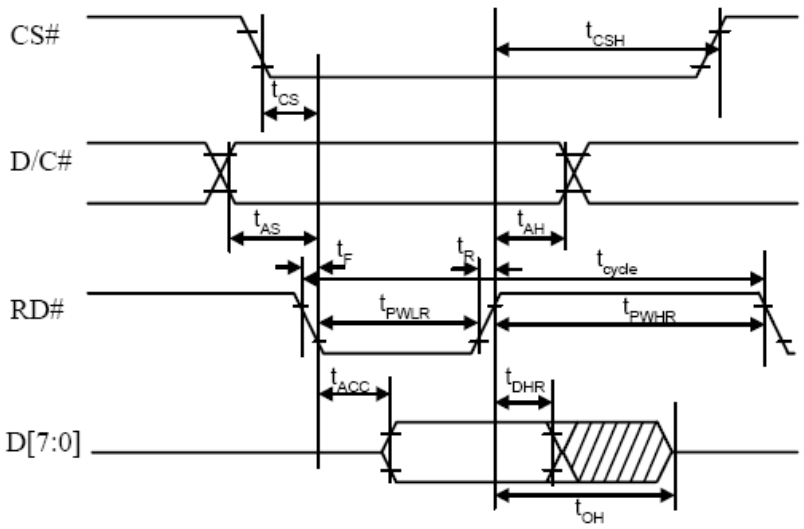
Notes:

VDD: 1.65V~3.3V
VCC_IN: 11.5~12.5V

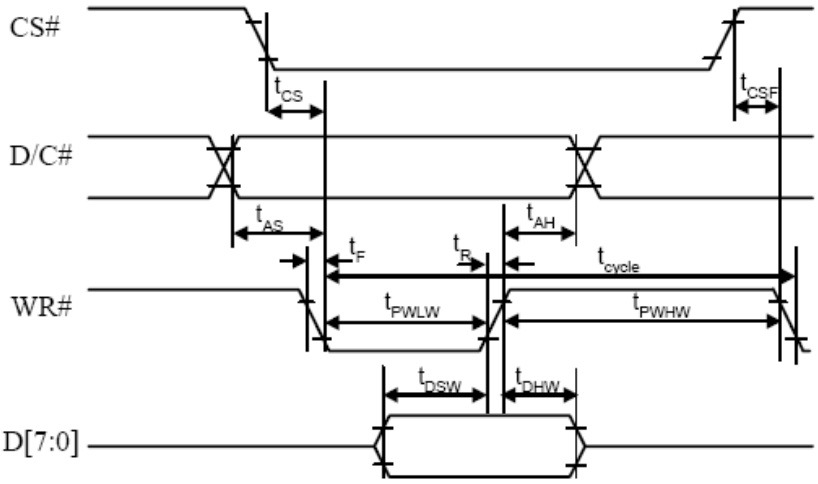
8.1.2 80XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
tcycle	Clock Cycle Time	300	-	ns
tAS	Address Setup Time	10	-	ns
tAH	Address Hold Time	0	-	ns
tDSW	Write Data Setup Time	40	-	ns
tDHW	Write Data Hold Time	7	-	ns
tDHR	Read Data Hold Time	20	-	ns
tOH	Output Disable Time	-	70	ns
tACC	Access Time	-	140	ns
tPWLR	Read Low Time	120	-	ns
tPWLW	Write Low Time	60	-	ns
tPWHR	Read High Time	60	-	ns
tPWHW	Write High Time	60	-	ns
tCS	Chip Select Setup Time	0	-	ns
tCSH	Chip Select Hold Time to Read Signal	0	-	ns
tCSF	Chip Select Hold Time	20	-	ns
tR	Rise Time	-	15	ns
tF	Fall Time	-	15	ns

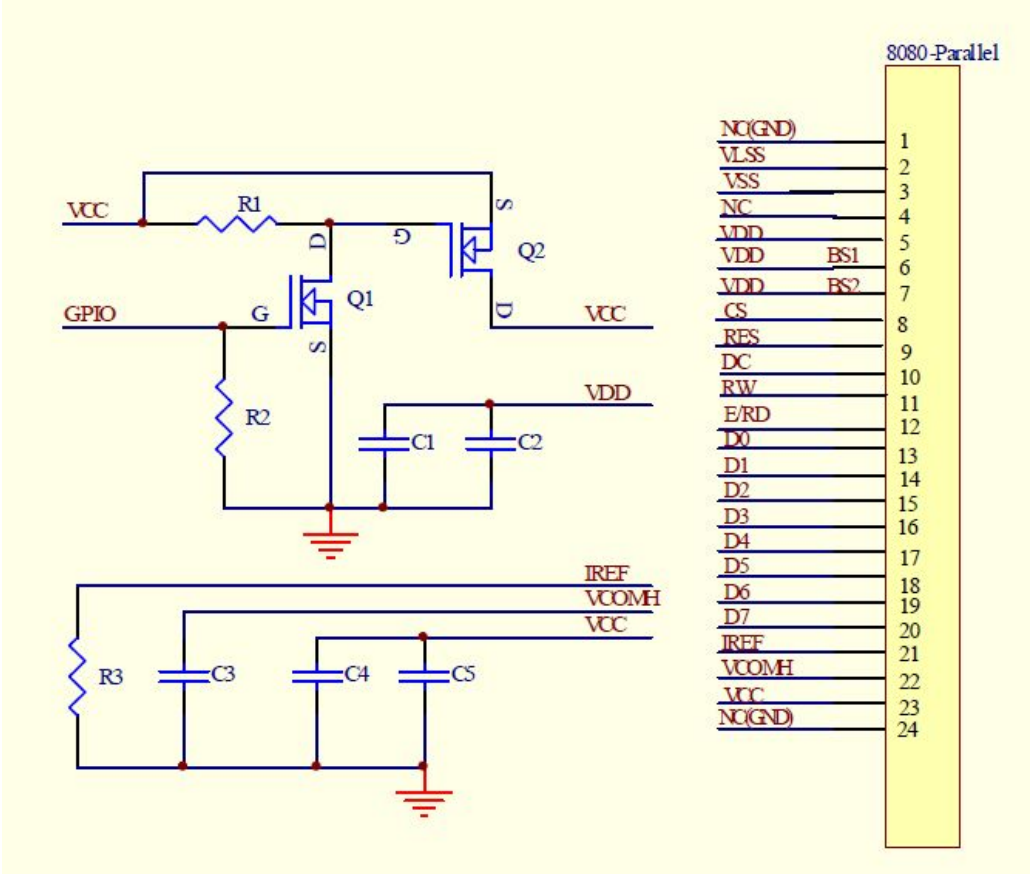
* (V_{DD} - V_{SS} = 1.65V to 3.3V, T_a = 25°C)



(Read Timing)



(Write Timing)



Recommended Components:

C1, C2: 1μF / 16V, X5R
C3: 2.2μF /25V
C4: 4.7μF / 25V, X7R
C5: 0.1μF/ 25V, X7R
R1, R2: 47kΩ
R3: 910KΩ, R3 = (Voltage at IREF - VSS) / IREF
Q2: FDN338P
Q1: FDN335N

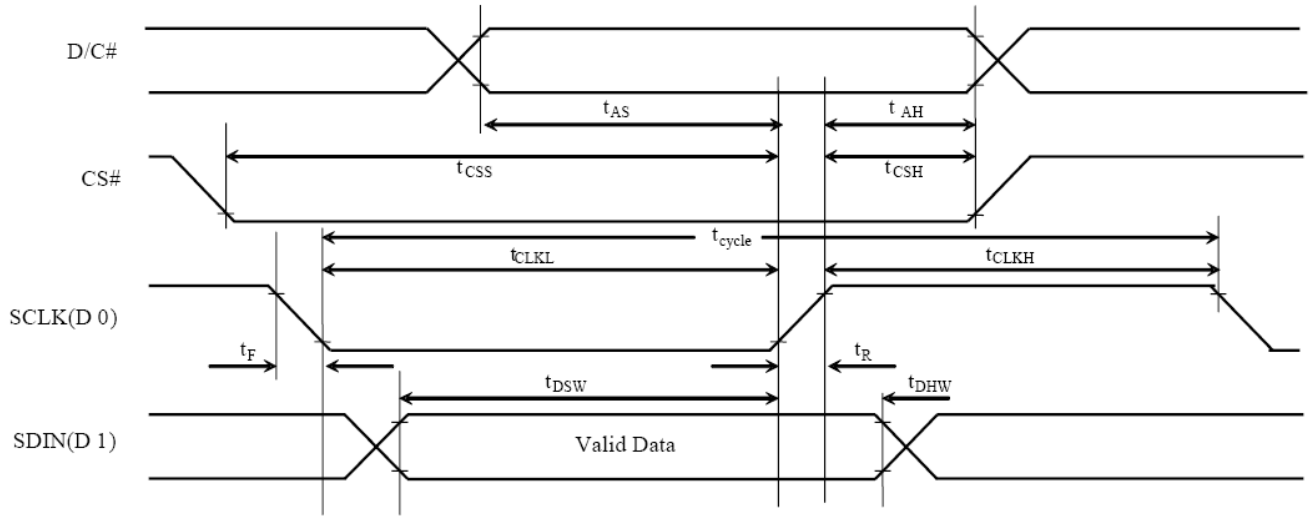
Notes:

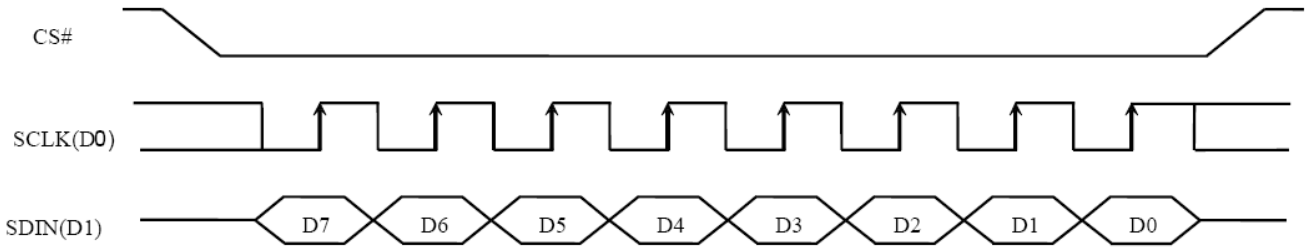
VDD: 1.65V~3.3V
VCC_IN: 11.5~12.5V

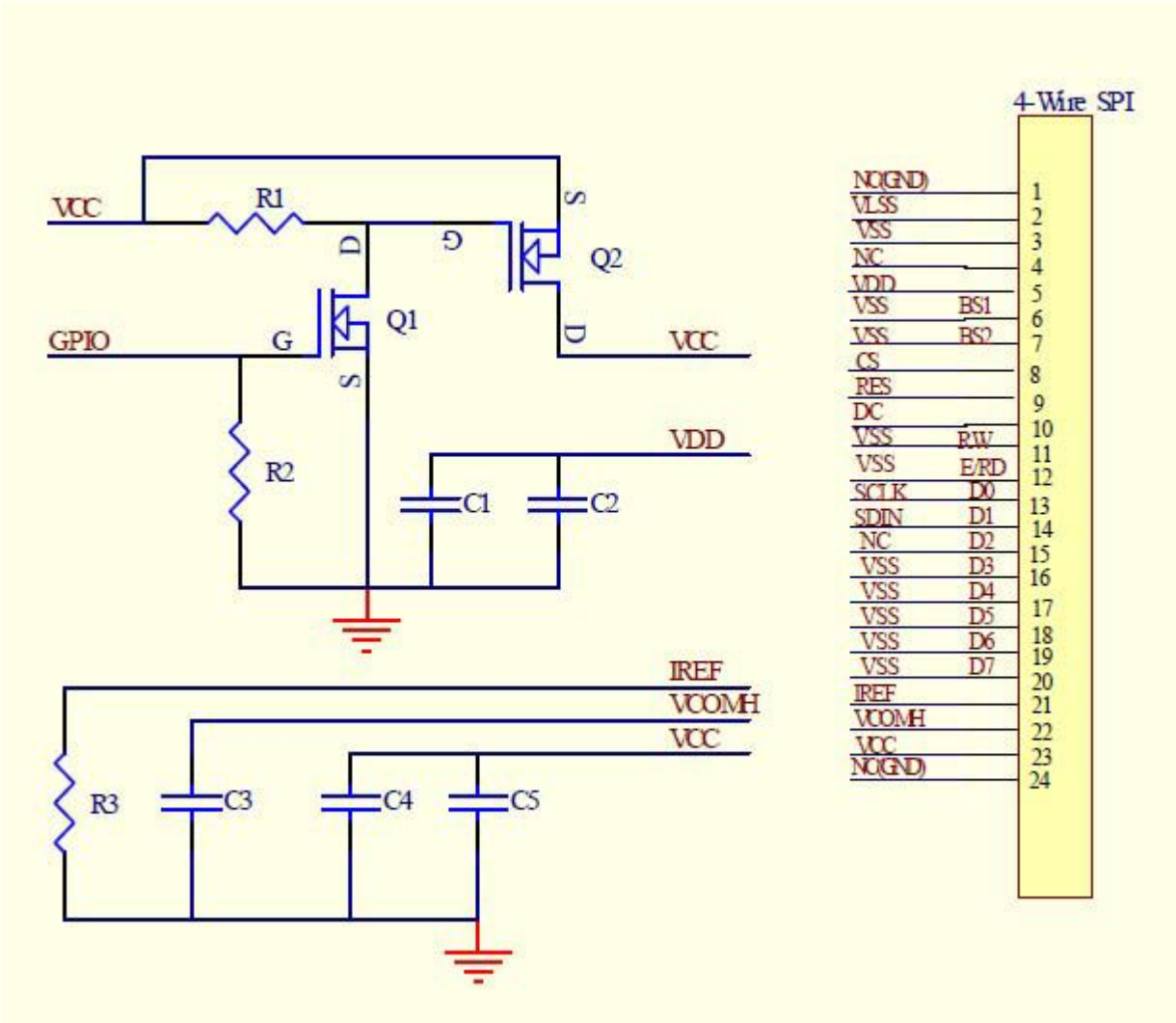
8.1.3 Serial Interface Timing Characteristics: (4-wire SPI)

Symbol	Description	Min	Max	Unit
tcycle	Clock Cycle Time	250	-	ns
tAS	Address Setup Time	150	-	ns
tAH	Address Hold Time	150	-	ns
tCSS	Chip Select Hold Time	120	-	ns
tCSH	Write Data Setup Time	60	-	ns
tDSW	Write Data Setup Time	50	-	ns
tDHW	Write Data Hold Time	15	-	ns
tCLKL	Serial Clock Low Time	100	-	ns
tCLKH	Serial Clock High Time	100	-	ns
tR	Rise Time	-	15	ns
tF	Fall Time	-	15	ns

* (V_{DD} - V_{SS} = 1.65V to 3.3V, T_a = 25°C)







Recommended Components:

C1, C2: 1μF / 16V, X5R
C3: 2.2μF /25V
C4: 4.7μF / 25V, X7R
C5: 0.1μF/ 25V, X7R
R1, R2: 47kΩ
R3: 910KΩ, R3 = (Voltage at IREF - VSS) / IREF
Q2: FDN338P
Q1: FDN335N

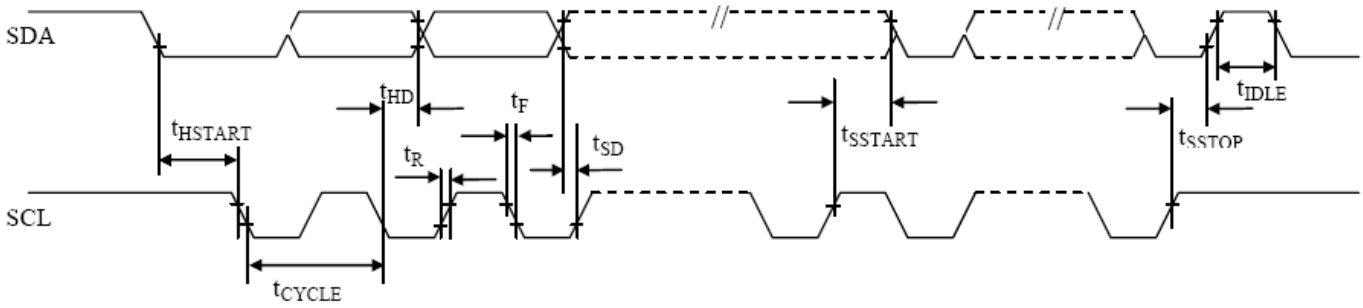
Notes:

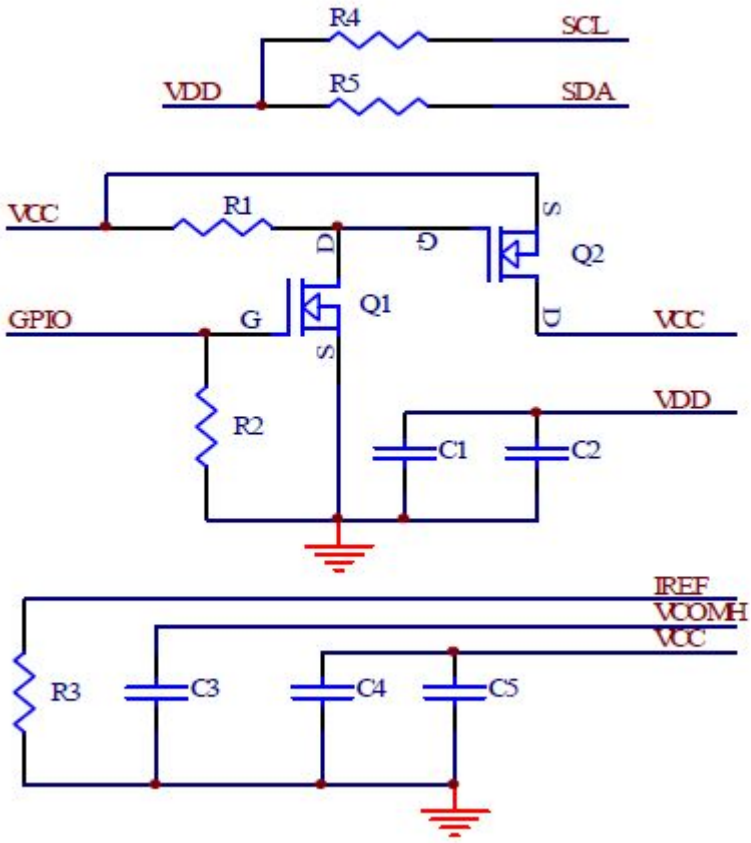
VDD: 1.65V~3.3V
VCC_IN: 11.5~12.5V

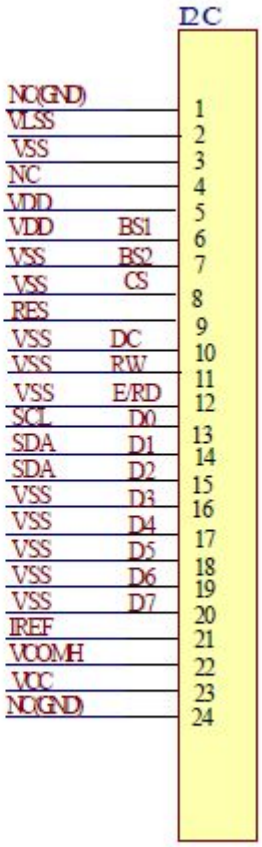
8.1.4 I2C Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
tcycle	Clock Cycle Time	2.5	-	us
tHSTART e	Start Condition Hold Tim	0.6	-	us
tHD	Data Hold Time (for “SDAOUT” Pin)	0	-	ns
	Data Hold Time (for “SDAIN” Pin)	300	-	ns
tSD	Data Setup Time	100	-	ns
tSSTART	Start Condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	us
tSSTOP	Stop Condition Setup Time	0.6	-	us
tR	Rise Time for Data and Clock Pin		300	ns
tF	Fall Time for Data and Clock Pin		300	ns
tIDLE	Idle Time before a New Transmission can Start	1.3	-	us

* (V_{DD} - V_{SS} = 1.65V to 3.3V, T_a = 25°C)







Recommended Components:

C1, C2: 1μF / 16V, X5R
C3: 2.2μF /25V
C4: 4.7μF / 25V, X7R
C5: 0.1μF/ 25V, X7R
R1, R2: 47kΩ
R3: 910KΩ, R3 = (Voltage at IREF - VSS) / IREF
R4, R5: 4.7kΩ
Q2: FDN338P
Q1: FDN335N

Notes:

VDD: 1.65V~3.3V
VCC_IN: 11.5~12.5V

The I2C slave address is 0111100b'. If the customer ties D/C# to VDD, the I2C slave address will be 0111101b'.

8.2. Functional Specification

8.2.1 Commands

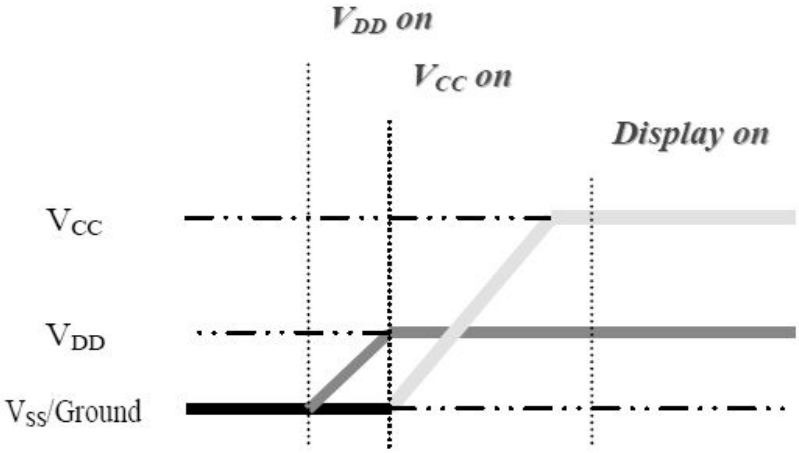
Refer to the Technical Manual for the SPD0301

8.2.2 Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

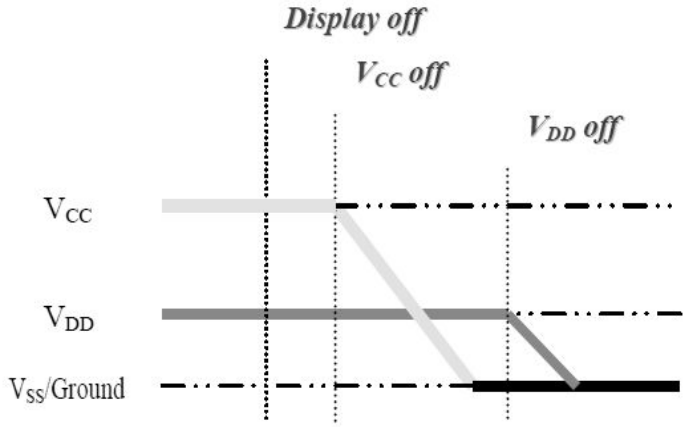
8.2.2.1. Power up Sequence:

1. Power up VDD
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up VCC
6. Delay 100ms (When VCC is stable)
7. Send Display on command



8.2.2.2 Power down Sequence:

1. Send Display off command
2. Power down VCC
3. Delay 100ms (When VCC is reach 0 and panel is completely discharges)
4. Power down VDD



Note :

1) Since an ESD protection circuit is connected between VDD and VCC inside the driver IC, VCC becomes lower than VDD whenever VDD is ON and VCC is OFF.
2) VCC should be kept float (disable) when it is OFF.
3) Power Pins (VDD, VCC) can never be pulled to ground under any circumstance.
4) VDD should not be power down before VCC power down.

8.3 Reset Circuit

When RES# input is low, the chip is initialized with the following status:

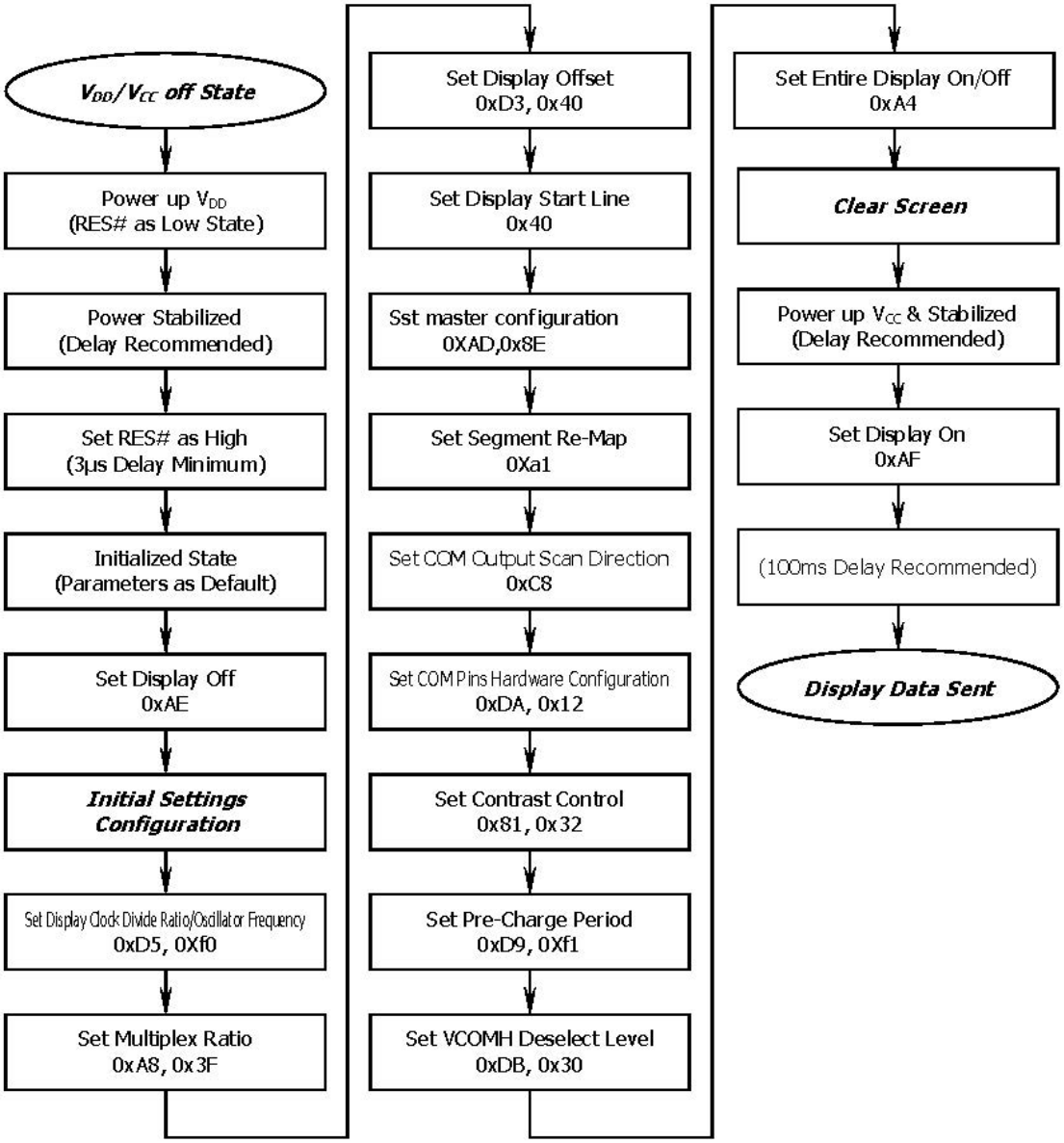
1. Display is OFF
2. 128 64 Display Mode
3. Normal segment and display data column and row address mapping (SEG0 mapped to column address 00h and COM0 mapped to row address 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 7Fh
9. Normal display mode (Equivalent to A4h command)

8.4 Actual Application Example

Command usage and explanation of an actual example

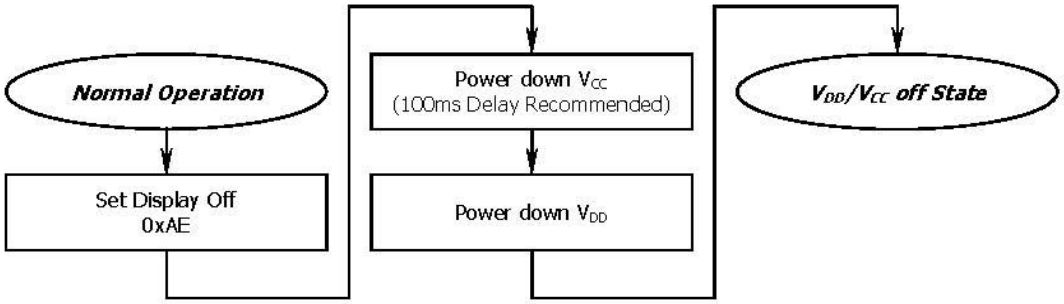
VCC Supplied Externally

<Power up Sequence>

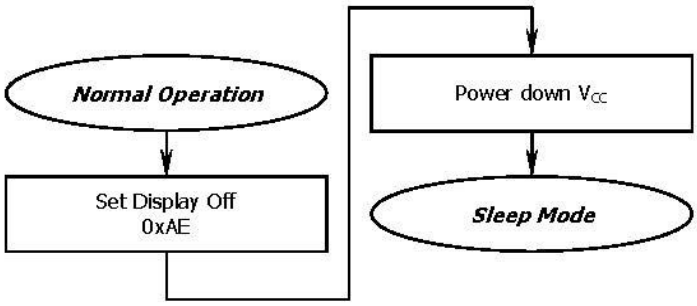


If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

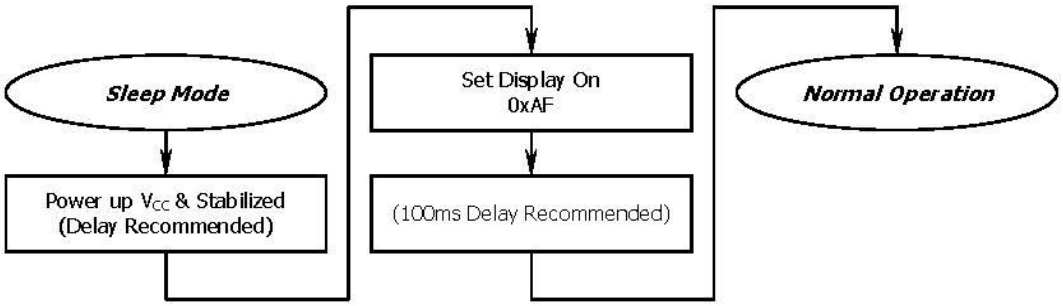
<Power down Sequence>



<Entering Sleep Mode>



<Exiting Sleep Mode>



External setting

```
void SPD0301 ()
{
      RES=0;
      delay(1000);
      RES=1;
      delay(1000);
      write_i(0xae); /* set display off */
      write_i(0x00); /* set lower column start address */
      write_i(0x10); /* set higher column start address */
      write_i(0x40); /* set display start line */
      write_i(0x81); /* set contrast control */
      write_i(0x32);
      write_i(0xa1); /* set segment remap */
      write_i(0xa6); /* set normal display */
      write_i(0xa8); /* set multiplex ratio */
      write_i(0x3f); /* 1/64 */
```

```
    write_i(0xc8); /* set com scan direction */
    write_i(0xd3); /* set display offset */
    write_i(0x00);
    write_i(0xd5); /* set display clock divide/oscillator frequency */
    write_i(0xa0);
    write_i(0xD9);
    write_i(0xF1);
    write_i(0xda); /* set com pin configuartion */
    write_i(0x12);
    write_i(0x91);
    write_i(0x3F);
    write_i(0x3F);
    write_i(0x3F);
    write_i(0x3F);
    write_i(0xaf); /* set display on */
}

void write_i(unsigned char ins)
{
    RS=0;
    CS=0;
    WR=0;
    P1=ins;
    WR=1;
    CS=1;
}

void write_d(unsigned char dat)
{
    RS=1;
    CS=0;
    WR=0;
    P1=dat;
    WR=1;
    CS=1;
}

void delay(unsigned int i)
{
    while(i>0)
     {
        i--;
     }
}
```

9. Optical Specification

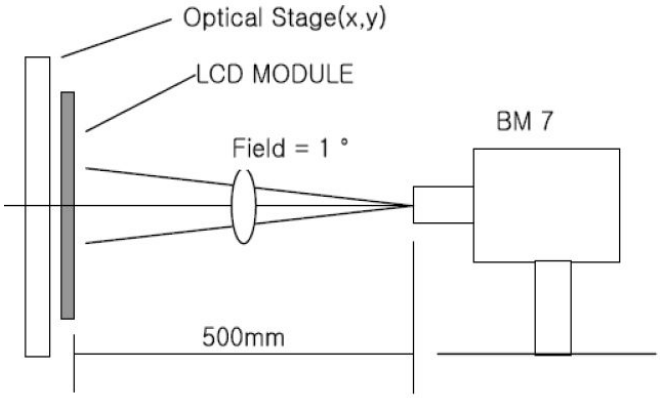
Ta=25℃

Item		Symbol	Condition	Min	Typ.	Max.	Unit	Remark
Contrast Ratio		CR	θ=0°		>2000:1	-		Note1 Note2
View Angles		Θ	--	>160		-	Degree	Note 3
Chromaticity	white	x	Without Polarizer	0.24	0.28	0.32		Note4, Note1
		y		0.28	0.32	0.36		
Luminance		L	With Polarizer	90	110	-	cd/m^2	Note1 Note5

Note 1: Definition of optical measurement system.

Temperature = 25℃(±3℃)

LED back-light: ON, Environment brightness < 150 lx

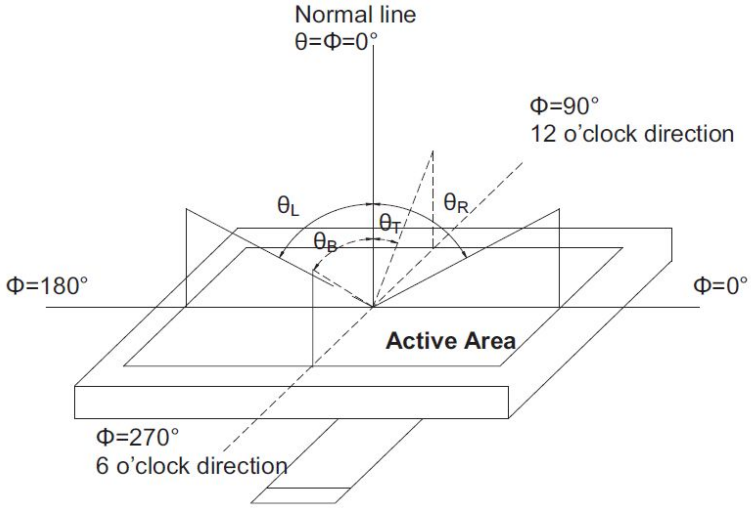


Note 2: Contrast ratio is defined as follow:

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

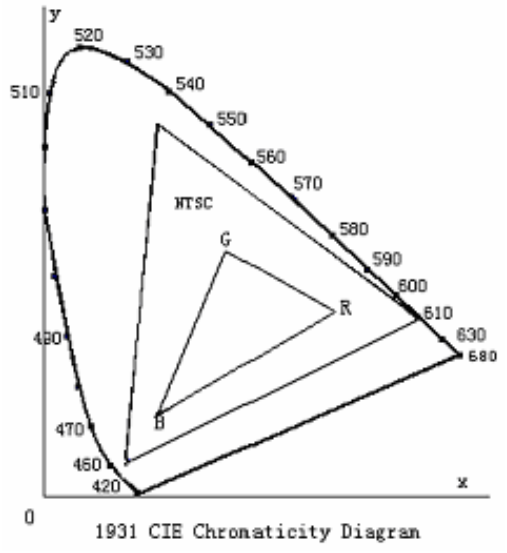
Note 3: Viewing angle range is defined as follow:

Viewing angle is measured at the center point of the OLED.



Note 4: Color chromaticity is defined as follow: (CIE1931)

Color coordinates measured at center point of OLED.



$$S = \frac{\text{area of RGB triangle}}{\text{area of NTSC triangle}} \times 100\%$$

Note 5: Luminance is defined as follow:

Luminance is defined as the brightness of all pixels “White” at the center of display area on optimum contrast.

10. Environmental / Reliability Tests

No	Test Item	Condition	Judgment criteria
1	High Temp Operation	Ts=+70℃, 120hrs	Per table in below
2	Low Temp Operation	Ta=-40℃, 120hrs	Per table in below
3	High Temp Storage	Ta=+85℃, 120hrs	Per table in below
4	Low Temp Storage	Ta=-40℃,120hrs	Per table in below
5	High Temp & High Humidity Storage	Ta=+65℃, 90% RH 120 hours	Per table in below (polarizer discoloration is excluded)
6	Thermal Shock (Non-operation)	-40°C ~85°C (-40°C /30min; transit /3min; 85°C /30min; transit/3min) 1cycle: 66min, 100 cycles	Per table in below
7	ESD (Operation)	C=150pF, R=330Ω， 5points/panel Air:±8KV, 5times; Contact:±4KV, 5 times;	Per table in below
8	Vibration (Non-operation)	Frequency range:10~55Hz, Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z.	Per table in below
9	Shock (Non-operation)	60G 6ms, ±X,±Y,±Z 3times, for each direction	Per table in below
10	Package Drop Test	Height:80 cm, 1 corner, 3 edges, 6 surfaces	Per table in below

INSPECTION	CRITERION(after test)
Appearance	No Crack on the FPC, on the OLED Panel
Alignment of OLED Panel	No Bubbles in the OLED Panel No other Defects of Alignment in Active area
Electrical current	Within device specifications
Function / Display	No Broken Circuit, No Short Circuit or No Black line No Other Defects of Display

11. Precautions for Use of OLED Modules

11.1 Safety

The liquid crystal in the OLED is poisonous. Do not put it in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and water.

11.2 Handling

A. The OLED and touch panel is made of plate glass. Do not subject the panel to mechanical shock or to excessive force on its surface.
B. Do not handle the product by holding the flexible pattern portion in order to assure the reliability
C. Transparency is an important factor for the touch panel. Please wear clear finger sacks, gloves and mask to protect the touch panel from finger print or stain and also hold the portion outside the view area when handling the touch panel.
D. Provide a space so that the panel does not come into contact with other components.
E. To protect the product from external force, put a covering lens (acrylic board or similar board) and keep an appropriate gap between them.
F. Transparent electrodes may be disconnected if the panel is used under environmental conditions where dew condensation occurs.
G. Property of semiconductor devices may be affected when they are exposed to light, possibly resulting in IC malfunctions.
H. To prevent such IC malfunctions, your design and mounting layout shall be done in the way that the IC is not exposed to light in actual use.

11.3 Static Electricity

A. Ground soldering iron tips, tools and testers when they are in operation.
B. Ground your body when handling the products.
C. Power on the OLED module before applying the voltage to the input terminals.
D. Do not apply voltage which exceeds the absolute maximum rating.
E. Store the products in an anti-electrostatic bag or container.

11.4Storage

A. Store the products in a dark place at +25℃±10℃ with low humidity (40% RH to 60% RH). Don't expose to sunlight or fluorescent light.
B. Storage in a clean environment, free from dust, active gas, and solvent.

11.5 Cleaning

A. Do not wipe the touch panel with dry cloth, as it may cause scratch.
B. Wipe off the stain on the product by using soft cloth moistened with ethanol. Do not allow ethanol to get in between the upper film and the bottom glass. It may cause peeling issue or defective operation. Do not use any organic solvent or detergent other than ethanol.

11.6 Cautions for installing and assembling

Bezel edge must be positioned in the area between the Active area and View area. The bezel may press the touch screen and cause activation if the edge touches the active area. A gap of approximately 0.5mm is needed between the bezel and the top electrode. It may cause unexpected activation if the gap is too narrow. There is a tolerance of 0.2 to 0.3mm for the outside dimensions of the touch panel and tail. A gap must be made to absorb the tolerance in the case and connector.